

(Senior) ASIC Analog Design Engineer (m/f/d) - REF5389A

工作职责

As an (Senior) ASIC Analog Design Engineer (m/f/diverse) for AESS (Advanced Electronics & Semiconductor Solutions), you will lead the development of analog and mixed-signal high-voltage integrated circuits for automotive applications, such as sensor interfaces and smart power devices. You will be responsible for complex transistor level analog designs, analog-on-top integration, requirements breakdown, mentoring junior engineers and chip top-level integration. Your work will directly contribute to the safety, efficiency, and innovation of next-generation automotive systems.

Tasks:

- Act as a key technical interface, coordinating with multidisciplinary teams—including system architects, digital designers, verification engineers, layout specialists, and test engineers—to ensure optimal design trade-offs and successful project execution.
- Define and implement analog blocks in BCD technologies, such as SMPSs, LDOs, Gate Drivers, Charge Pumps
- Perform requirements breakdown from system-level specifications to block-level design targets
- Discuss, negotiate and investigate chip requirements with internal customers
- Collaborate with digital design, layout, verification, and test teams to ensure seamless integration
- Perform chip-top level integration

职位要求

- Academic degree in electrical engineering, microelectronics, physics or comparable qualification
- Senior-level of experience in analog/mixed-signal high-voltage, high-power ASIC design in the automotive domain
- Good understanding of BCD technologies
- Proven track record of tape-outs and successful silicon validation
- Knowledge of functional safety and reliability engineering
- Exposure to EMC/ESD design and robustness testing
- Strong understanding of analog circuit theory, and physical layout considerations
- Experience with analog-on-top simulation environments and mixed-signal verification
- Familiarity with automotive-grade design constraints and qualification processes
- Very good English language skills (both written and spoken), German language skills desirable
- Ability to take initiative and to communicate effectively
- Eagerness to grow and develop

Applications from severely handicapped people are welcome.



职位号码

REF5389A

工作职能

工程

所在地

Regensburg

领导力级别

个人贡献者

招聘专员

Daniela Krebs

法律实体名称

AUMOVIO Germany GmbH

我们可以提供

- Next to the interesting daily work, the region around Regensburg is offering a high recreational value and quality of life.
- Profit from extensive benefits at the location such as different canteens and cafeterias, a continuing education and training, health management, physiotherapy and much more.
- We offer an attractive salary as well as the possibility of hybrid and cross-border mobile work.
- For an improved work-life balance we support you with various initiatives for a better compatibility of family and career such as flexible work time model, part-time option, sabbatical, etc.
- You can expect a highly motivated team, as well as diverse topics and projects in the global environment of the automotive industry.
- We are promoting lifelong learning combined with personal and professional development.
- You are looking for an individual working time model? We support part-time work.

Ready to take your career to the next level? The future of mobility isn't just anyone's job. Make it yours! **Join AUMOVIO. Own What's Next.**

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关于我们

At AUMOVIO, we own what we do: Developing and producing hardware, software, and services that shape the future of mobility. But what truly sets us apart are our people. People who thrive in our winning culture, driven by bold ideas. People who take a leap and create meaningful difference—together. Because we believe that the future belongs to those who own it. That's why we foster a culture where you own every step of the way.

Own your career, your growth, your skills, and your impact. Join us and own what's next.

Advanced Electronics & Semiconductor Solutions (AESS) organization has been established in AUMOVIO to develop and manufacture semiconductors in a fabless model to fulfilling strategic internal semiconductor demands.