

IC Verification Engineer

Vaše náplň práce

Detailed task description

- Collect, discuss and evaluate requirements related to IC test & validation concept(s) in cooperation with other disciplines' developers
- Actively support system and/or IC concept and architecture definition, considering feasibility with semiconductor technologies and test strategy
- Apply new validation concepts to the design verification.
- Define requirements of the IC validation together in cooperation with other disciplines' developers
- Specify IC validation characteristics and interfaces within component specification document
- Responsible for the technical communication with the ASIC supplier during the whole ASIC development
- Judge and approve simulation/design results in consideration of defined system requirements
- Decide on optimal IC verification concept based on simulation results and worst-case calculations
- Evaluate technical and development risks for IC development together with ASIC PM
- Plan time schedule for dedicated ASIC project tasks, track validation progress, perform bench tests
- Create and maintain development documents
- Apply configuration and change management, apply quality assurance management
- From circuits specifications, ASIC verification engineer should specify verification strategies and testbench architectures (SystemVerilog, UVM, C-driven, others) to ensure optimum verification coverages
- Elaborate detailed verification plans corresponding to circuit specifications
- Develop verification environments and tests/sequences according to verification plans
- Responsible of the definition of the verification strategies, of their implementation and of the verification quality
- Improve the verification flow
- He is responsible for carrying out all assigned tasks with a focus on function, quality, test architecture, test coverage, schedule, and delivery of verification in time.
- Together with other disciplines' developers, the verification engineer is defining integration concepts, specifying the IC test requirements, defining related test architecture, and verifying implemented functions. The is taking care about process implementation and schedule
- IC (ASIC) Verification The engineer is responsible for developing functional models for Analog and/or Digital IPs. Developing Digital and analog/mixed-signal test benches, Interaction between IPs at chip level (analog and digital), developing test benches, Functional

ID pracovní pozice
REF4569M

Lokalita
Bengaluru

Úroveň vedení lidí
Vedení sebe

Právnícká osoba
**Continental Automotive
Components Private Ltd.**

verification, Technical support of co-workers and IP designers,
Provide technical support to test engineers

Váš profil

- Master of Science in Electrical Engineering/Microelectronics/ VLSI design or similar qualification.
- Bachelor of science with advanced course in VLSI Design.

Co nabízíme

REQUIRED KNOWLEDGE

- * Organizational Standard Process and Methods (Risk Management, Project Management..)
- * Knowledge of test tools, automation
- * System Requirements
- * System Architecture
- * Functional Safety Management (ISO26262)
- * System Security & Privacy Engineering (UNECE WP29)
- * Communication
- * Knowledge of test process, test methods, techniques and tools
- * Capability to analyse and solve problems
- * Product knowledge (for his responsibility)

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O nás

Since its spin-off in September 2025 AUMOVIO continues the business of the former Continental group sector Automotive as an independent company. The technology and electronics company offers a wide-ranging portfolio that makes mobility safe, exciting, connected, and autonomous. This includes sensor solutions, displays, braking and comfort systems, as well as comprehensive expertise in software, architecture platforms, and assistance systems for software-defined vehicles. In the fiscal year 2024, the business areas, which now belong to AUMOVIO, generated sales of 19.6 billion euro. The company is headquartered in Frankfurt, Germany, and has about 87,000 employees in more than 100 locations worldwide.